AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1 (currently amended). A playback method for a recording medium to which data is recorded in block units containing multiple fixed-length frames ~~together with~~ , and block address information is pre-recorded, the playback method comprising ~~steps of~~ :

acquiring the data ~~and the block address information~~ from a first playback signal from the recording medium;

acquiring the block address information from a second playback signal based on pre-recorded block address information from the recording medium;

predicting the recording position of each frame in a block from the acquired block address information;

synchronizing to [[the]] a frame level based on the acquired data;

determining the memory address for storing the data acquired based on the predicted recording position; and

storing the acquired data at the determined memory address.

2 (currently amended). A playback method for a recording medium according to claim 1, further comprising ~~steps of~~ :

determining whether synchronization at the data frame unit level has been established; and

detecting whether synchronization at the frame unit has been restored if frame synchronization goes out-of-step [[;]] ,

wherein when recovery of frame synchronization is detected, the memory address to which data is stored is determined based on the predicted frame recording position.

3 (original). A playback method for a recording medium according to claim 1, wherein the data memory address in memory is determined with the frame as the smallest recordable unit.

4 (original). A playback method for a recording medium according to claim 1, wherein block address information is recorded to the recording medium in a format different from the data recording format.

5 (currently amended). A playback method for a recording medium according to claim 1, further comprising ~~steps of~~ :

generating a result information for detection of synchronization code coded at the frame unit level according to specific rules;

demodulating the data in each frame to demodulated frame data; and

adding to each demodulated frame data block the result information for detection of synchronization code correlated to each frame.

6 (currently amended). A playback method for a recording medium according to claim 1, further comprising ~~a step of~~ synchronizing at the frame unit level based on the acquired address information.

7 (currently amended). A playback control circuit for a recording medium to which data is recorded in block units containing multiple fixed-length frames ~~together with~~ , and block address information is pre-recorded, comprising:

a signal ~~reading means for acquiring~~ reader that acquires the data from a first playback signal from the recording medium, and acquires [[and]] the block address information from a second playback signal based on pre-recorded block address information from the recording medium;

a recording address ~~predicting means for predicting~~ predictor that predicts the recording position of each frame in a block from the acquired block address information;

a synchronizer that synchronizes ~~synchronization means for synchronizing~~ to the frame level based on the acquired data;

a memory ~~for storing~~ that stores the data; and

a controller that determines ~~control means for determining~~ the memory address for storing data based on the predicted recording position.

8 (currently amended). A playback control circuit according to claim 7, further comprising a synchronization ~~detection means for determining~~ detector that determines

whether synchronization at the data frame unit level has been established, and ~~detecting~~ detects whether synchronization at the frame unit has been restored if frame synchronization goes out-of-step [[;]] .

wherein the ~~control means~~ controller determines the memory address to which data is stored based on the recording position predicted by the recording address ~~predicting means~~ predictor when the synchronization ~~detection means~~ detector detects recovery of frame synchronization.

9 (currently amended). A playback control circuit according to claim 7, wherein ~~the~~ a data memory address in memory is determined with the frame as the smallest recordable unit.

10 (original). A playback apparatus for a recording medium to which data is recorded in block units containing multiple fixed-length frames together with block address information, comprising the playback control circuit according to claim 7.

11 (currently amended). A playback method for reproducing data from a recording medium to which is recorded modulated frame data and a specific synchronization code prepended to the beginning of the modulated frame data,

the modulated frame data being error correction coded data segmented into multiple frame data blocks of a specific length and then modulated,

the playback method comprising ~~steps of~~ :

acquiring signals from the recording medium;

acquiring a detection result of synchronization code by detecting frame synchronization codes from the acquired signals;

correcting frame synchronization based on the result for detection of acquired synchronization code;

generating a result information for detection of synchronization code coded according to specific rules from the detection result of synchronization code;

demodulating the modulated frame data for each frame and generating demodulated frame data; [[and]]

adding the result information for detection of synchronization code for each frame to the corresponding demodulated frame data [[.]] ; and

rectifying an error according to the detected synchronization code.

12 (currently amended). A playback method according to claim 11, ~~further comprising~~ wherein rectifying an error comprises:

~~a erasure pointer generating step for~~ generating [[a]] an erasure pointer for ~~erasure correction~~ erasure-correction based on the demodulated frame data using the corresponding result information for detection of synchronization code; and

~~an error correcting step for erasure correcting~~ erasure-correction error correcting code from multiple demodulated frame data blocks using the erasure pointers for the demodulated frame data.

13 (currently amended). A playback method according to claim 11, further comprising:

a memory ~~step for storing~~ that stores the result information for detection of synchronization code and corresponding demodulated frame data in different memory areas with a known correlation therebetween.

14 (currently amended). A playback method according to claim 11, wherein the result information for detection of synchronization code is coded to differentiate between at least [[the]] three detection results of "normal detection" when the synchronization code is detected normally, "undetected" when the synchronization code is not detected, and "out-of-step synchronization" when a next synchronization code is detected at a timing offset from a timing predicted from the timing of the detection result for the previously detected synchronization code.

15 (currently amended). A playback method according to claim 11, wherein when [[the]] correcting frame synchronization [[step]] corrects synchronization delay in which a new synchronization code is detected earlier than the timing predicted from the timing of the detection result of the previously detected synchronization code, and the synchronization delay is less than one frame,

the memory [[step]] corrects the memory address of the frame data immediately after synchronization delay correction to an address derived by skipping an amount

equivalent to the synchronization delay correction, and stores the frame data to the corrected address.

16 (currently amended). A playback method according to claim 15, wherein when [[the]] correcting frame synchronization [[step]] corrects synchronization delay in which a new synchronization code is detected earlier than the timing predicted from the timing of the previously detected synchronization code, and the synchronization delay is greater than or equal to one frame,

the memory [[step]] corrects the memory address of the result information for detection of synchronization code and frame data immediately after synchronization delay correction to an address shifted equivalently to the correction for the synchronization delay, and then stores the data to the corrected address; and

[[the] an erasure pointer ~~generating step~~ generator determines that result information for detection of synchronization code that is skipped and not stored to memory was undetected, and generates [[a]] an erasure pointer thereto.

17 (currently amended). A playback control circuit for reproducing data from a recording medium to which is recorded modulated frame data and a specific synchronization code prepended to the beginning of the modulated frame data,

the modulated frame data being error correction coded data segmented into multiple frame data blocks of a specific length and then modulated,

the playback control circuit comprising:

a frame ~~synchronization means for correcting~~ synchronizer that corrects frame synchronization based on a detection result of synchronization code acquired by detecting frame synchronization codes from playback signals acquired from the recording medium;

a ~~generating means for generating~~ generator that generates a result information for detection of synchronization code coded according to specific rules from the detection result of synchronization code;

a ~~demodulation means for demodulating~~ demodulator that demodulates the modulated frame data for each frame and generating demodulated frame data;

an ~~adding means for prepending~~ adder that prepends the result information for detection of synchronization code for a frame to the beginning of the demodulated frame data;

a memory ~~for storing~~ that stores the result information for detection of synchronization code and demodulated frame data; [[and]]

a memory ~~control means for storing~~ controller that stores the result information for detection of synchronization code and demodulated frame data to memory [[.]] ; and

a rectifier that rectifies an error according to the detected synchronization code.

18 (currently amended). A playback control circuit according to claim 17, further comprising:

an erasure pointer ~~generating means for generating a~~ generator that generates an erasure pointer for ~~erasure correction~~ erasure-correction using the result information for detection of synchronization code; and

an error ~~correcting means for erasure correcting~~ corrector that erasure-corrects error correcting code composed from demodulated frame data using the erasure pointers.

19 (currently amended). A playback control circuit according to claim 17, wherein the memory ~~control means~~ controller stores the result information for detection of synchronization code and demodulated frame data to different memory areas.

20 (currently amended). A playback control circuit according to claim 17, wherein the result information for detection of synchronization code is coded to differentiate between at least [[the]] three detection results of "normal detection" when the synchronization code is detected normally, "undetected" when the synchronization code is not detected, and "out-of-step synchronization" when a next synchronization code is detected at a timing offset from a timing predicted from the timing of the detection result for the previously detected synchronization code.

21 (currently amended). A playback control circuit according to claim 17, wherein when the frame synchronization means corrects synchronization delay in which a new synchronization code is detected earlier than the timing predicted from the timing of the previously detected synchronization code, and the synchronization delay is less than one frame,

the memory ~~control means~~ controller corrects the memory address of the frame data immediately after synchronization delay correction to an address derived by

skipping an amount equivalent to the synchronization delay correction, and stores the frame data to the corrected address.

22 (currently amended). A playback control circuit according to claim 21, wherein when the frame ~~synchronization means~~ synchronizer corrects synchronization delay in which a new synchronization code is detected earlier than the timing predicted from the timing of the previously detected synchronization code, and the synchronization delay is at least ~~greater than or~~ equal to one frame,

the memory ~~control means~~ controller corrects the memory address of the result information for detection of synchronization code and frame data immediately after synchronization delay correction to an address shifted equivalently to the correction for synchronization delay, and then stores the frame data to the corrected address; and

the erasure pointer ~~generating means~~ generator determines that result information for detection of synchronization code correspond to a frame that is skipped and not stored to memory was undetected, and generates a erasure pointer thereto.

23 (original). A playback apparatus for reproducing data from a recording medium to which is recorded modulated frame data and a specific synchronization code prepended to the beginning of the modulated frame data,

the modulated frame data being error correction coded data segmented into multiple frame data blocks of a specific length and then modulated,

the playback apparatus comprising the playback control circuit according to claim 17.